Journal of
Electrical & Electronic Systems

Jadeja et al., J Electr Electron Syst 2015, 4:2
DOI: 10.4172/2332-0796.1000148

Research Article Open Access

Analysis of Power Reduction Techniques used in Testing of VLSI Circuits

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Abstract

One of the most important parameter over the past decade in VLSI design is the Power dissipation during manufacturing test, as the circuit consume much more power during test than functional mode of operation. This paper presents analysis of low power testing techniques by which Power optimized test patterns are obtained. The compaction technique has been validated using benchmark examples, and it has been shown that average 33% of test patterns have been reduced by which power is minimized. Evaluation of various techniques under consideration in this paper is carried out by open source tool ATALANTA for test pattern generation and MATLAB for optimization.

Keywords: Test pattern; BIST (Built in Self-Test); Test data reordering; Test data compression

Introduction

Testing is a process which ensures that the response of each fabricated circuit is acceptable. Production of authentic VLSI circuits depends strongly on testing which eliminates various faults caused by the fabrication processes. Switching activity increases during testing of different circuits compared to the normal operation of the circuit which raises the power dissipation and hence may lead to lower circuit manufacturing yield and reliability [1]. Different prominent approaches for low power VLSI testing which are well proven and widely used are discussed in. Combining compaction and test vector ordering technique reduces power dissipation during testing of combinational and sequential VLSI circuits. Experimental results, using compact and non-compact test sets, have shown that compact test sets have similar power dissipation during testing different circuits with reduction in testing time and computational time when compared to non-compact test sets.

Test Pattern Generation

Test pattern generation is an important part of the VLSI testing flow that offers many possibilities that can be explored for reducing test power dissipation. The most significant advantage of reducing test power through low power test pattern generation is that this approach causes neither circuit overhead nor performance degradation. However, low-power test pattern generation is a technical field, in which many important factors in addition to the effect of test power reduction has to be considered. Such factors include test vector count inflation, potential fault coverage loss, increased test pattern generation time, compatibility with compressed scan testing and test generation flow modification as discussed in. Low power Automatic Test Pattern Generation (ATPG) is an advanced class of ATPG that targets.

Test power reduction in addition to fault sensing during test cube generation [2]. General test generation targets combinational and sequential circuits. The goal of general low-power test generation is to create a sequence of test vectors that cause a minimal number of transitions at inputs between any two consecutive cycles.

The Table 1 represents various benchmark circuits, taken from ISCAS'85 benchmark suite, used in this research work (Figure 1). Atalanta [3] is an open source tool used for Automatic Test pattern generation and Fault simulator. Test pattern generation results include circuit structure, ATPG parameters, test pattern and fault simulation.

Table 1 shows result of test pattern generation which includes the information about number of primary inputs, number of primary outputs, number of gates, logic level of circuit, fault coverage and numbers of test patterns.

Generated test pattern undergoes two different techniques which is test pattern compaction technique and test pattern reordering technique to obtain power optimized test patterns. Test pattern compaction technique removes the test cubes which are identical and reduces the test pattern volume whereas test pattern reordering technique reduces the switching between two patterns therefore the number of transition reduces. At the end compression bits are measured in percentage in the section IV.

Test Pattern Compaction Technique

The aim of test compaction is to cut down the number of final test vectors. Test power reduction can also be achieved through test pattern compaction. Compaction is the work of combining multiple test cubes into one if they are compatible. Two test cubes, c1 and c2, are said to be compatible if two corresponding bits in c1 and c2 do not have opposite logic values [4]. Conventionally, compaction is

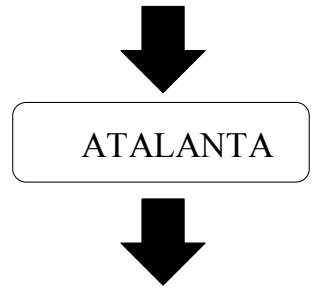

Figure 1: Atalanta Results.

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Received May 13, 2015; **Accepted** June 09, 2015; **Published** June 25, 2015

Citation: Jadeja SK, Patel R, Popat J (2015) Analysis of Power Reduction Techniques used in Testing of VLSI Circuits. J Electr Electron Syst 4: 148. doi:10.4172/2332-0796.1000148

Benchmark Circuit	Number of Primary Inputs	Number of Primary Output	Number of Gates	Logic Level of Circuit	Fault Coverage In %	Number of Test Patterns
C17	5	2	6	3	100	7
C432	36	7	160	17	99.237	69
C499	41	32	201	11	98.945	85
C880	60	26	383	24	100	98
C1355	41	32	546	24	99.492	110

Table 1: Test Pattern Generation For Different Bench Mark Circuits.

Benchmark circuit	Number of Test Pattern		Reduction in Test Patterns (%)
	Before Compaction	After Compaction	
C17	7	5	28.57
C432	69	46	33.33
C499	85	53	37.65
C880	98	57	41.83
C1355	110	84	23.64

Table 2: Test pattern compaction using atalanta.

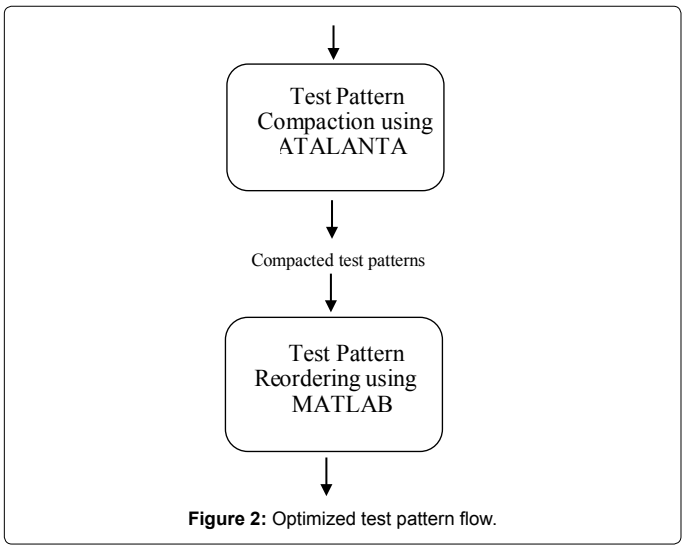

Figure 2: Optimized test pattern flow.

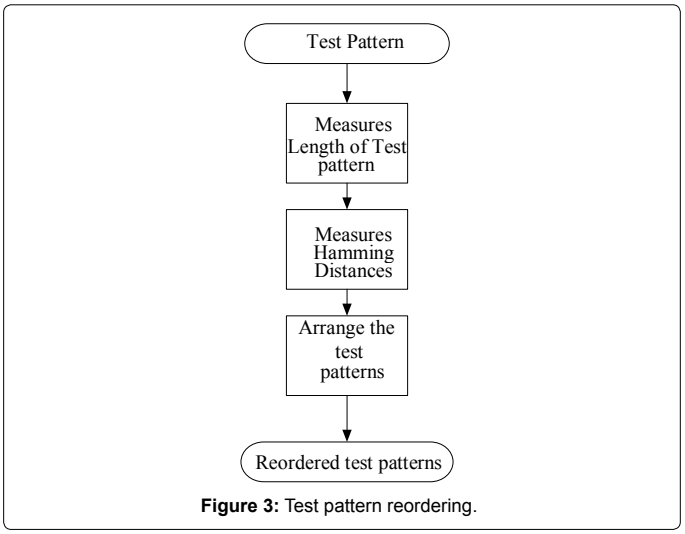

Figure 3: Test pattern reordering.

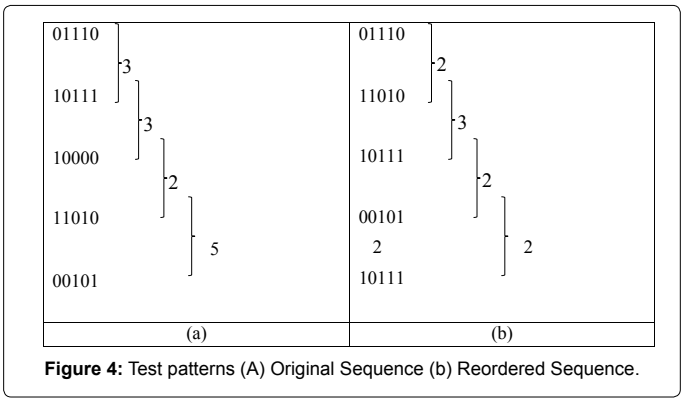

Figure 4: Test patterns (A) Original Sequence (b) Reordered Sequence.

conducted to reduce the final test vector count, it can also reduce test power if power is considered when compatible test cubes are merged. Compaction technique selects a target fault in such a manner that the risk of violating capture power limits is minimized [5].

Compaction of test patterns is done on different benchmark circuits using ATALANTA tool. Table 2 shows number of test patterns before and after compaction for each benchmark circuit.

Using test pattern compaction the average reduction of 33% in test patterns is observed. Test pattern reordering is done on compacted test vectors for reducing switching activity (Figure 2).

Test Pattern Reordering Technique

Test pattern reordering technique minimizes the number of transition between all the patterns. Reordering can be done using different algorithms like Shortest Path Algorithm, Traveling Salesman Problem (TSP), Simulated Annealing (SA), Hamming Distance, Genetic Algorithm (GA) [6], and Ant Colony Optimization [3].

In this paper Hamming distance based ordering is done for minimization of transition between test patterns. Reordering using hamming includes following steps which are demonstrated with example of C17 benchmark circuit (Figure 3).

Steps of Reordering [5,6] are given in Figure 4.

The example in Figure 4 shows the reduction in transition with the help of reordering. Test pattern of C17 benchmark circuit are reorder to minimize switching between test patterns.

As power is directly proportional to the switching activity as show in Equation, Power can be reduce by reducing switching (transition) between patterns.

$$P \alpha C V^2 \quad (1)$$

Where

α is Switching activity

C is capacitance

Benchmark circuit	Number of test pattern	Transition		Reduction in Transition (%)
		Before ordering	After ordering	
C17	5	13	9	30.77
C432	46	2961	1832	38.13
C499	53	1052	754	28.50
C880	57	7638	5498	28.02
C1355	84	16535	12457	24.66

Table 3: Results for reordering technique.

Benchmark circuit	Compressed Bits
C17	10
C432	828
C499	1312
C880	2460
C1355	1066

Table 4: compressed bits of different circuits.

V is Supply Voltage

After reordering the transitions of above test patterns are reduced from 13 to 9. Column wise ordering of test patterns is done in given example of Figure 4. Table 3 shows the experimental results of reordering technique applied on combinational benchmark circuits. Result shows that average reduction in transition is found 30%.

Test Pattern Compression

Test data compression technique is used to handle the problem of increased test data volume. The test data volume for manufacturing test of modern devices is increasing rapidly [7]. This is due to the facts that the transistor count for these chips is increasing exponentially and the use of advanced technology introduces new physical and timing related defects, which require new types of test. It is well known that power consumption during test is much higher than in the functional mode due to increased switching activity in test mode. Therefore, efficient techniques that minimize both test data volume and test power consumption are required. Techniques such as test data compression and built-in-self-test (BIST) are used commonly to handle the problem of increased test data volume.

Test compression call for compressing the number of test data (both input and response) that must be stored on automatic test equipment (ATE) for testing with a settled test set. This is done by adding some additional on-chip hardware before the scan chains to decompress the test stimulus coming from the ATE and after the scan chains to compress the response going to the ATE. This reduces amount of memory in ATE and even more importantly reduces test time because less data has to be transferred across the limited bandwidth between the ATE and the chip [8]. Moreover, test compression methodologies are easy to adopt in industry because they are compatible with the conventional design rules and test generation owns used for scan testing (Table 4). Test stimulus compression should be an information lossless procedure with respect to the specified (care) bits in order to preserve the fault coverage of the original test cubes. After decompression, the resulting test patterns shifted into the scan chains should match the original test cubes in all the specified (care) bits.

Conclusion

In this paper we have presented different power reduction techniques used during testing of VLSI circuits. This techniques is applied on test pattern to minimize test data volume and switching activity. Combining the different technique like compaction and test vector ordering technique, reduction in Power dissipation during testing combinational and sequential circuits. The proposed techniques better compression with no penalty in area and time. This techniques can be easily adopted for power reduction.

References

1. Girard P (2000) "Low Power Testing of VLSI Circuits: Problems and Solutions", Quality Electronic Design, IEEE First International Symposium.
2. Moorthy P, Bharathy SS (2013) "An efficient test pattern generator for high fault coverage in built-in-self-test applications" Fourth International Conference on Computing, Communications and Networking Technologies (ICCCNT) 1-4.
3. Wang J, Shao J, Li Y, Huang Y (2009) "Using Ant Colony Optimization for Test Vector Reordering", 2009 IEEE Symposium on Industrial Electronics and Applications (ISIEA 2009) 4-6.
4. Wu PH, Chen TT, Li WL, Rau JC (2008) "An Efficient Test-Data Compaction for Low Power VLSI Testing", Electro/Information Technology, IEEE International Conference.
5. Wu PH, Chen TT, Li WL, Rau JC (2008) "An efficient test-data compaction for low power VLSI testing" IEEE International Conference on Electro/Information Technology 237-241.
6. Mehta US, Devashrayee NM, Dasgupta KS (2010) "Hamming distance based 2D reordering with power efficient don't care bit filling: Optimizing the test data compression method." International Symposium on System-on-Chip Proceedings, SoC 1-7.
7. Hashempour H, Lombardi F (2004) "Compression of VLSI test data by arithmetic coding." IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems, DFT 2004. Proceedings: 150-157.
8. Roy S, Gupta I, Pal A (2208) "Artificial intelligence approach to test vector reordering for dynamic power reduction during VLSI testing." IEEE Region 10 Conference 1-6.